SEMICONDUCTOR PACKAGE WITHOUT SUBSTRATE AND METHOD OF MANUFACTURING SAME

FIELD OF THE INVENTION

This invention relates to a structure of semiconductor package without substrate and particularly a semiconductor package which has no substrate for reducing the package thickness and enhancing production yield and method of manufacturing same.

BACKGROUND OF THE INVENTION

The commonly used semiconductor packaging process generally includes the following steps: In dicing saw process, the wafer was cut into individual chip by means of wafer dicing machines according to a preset integrated circuit (IC) street mapped on the wafer; In die bonding process, the chip was mounted on a prefabricated lead frame or substrate; In wire bonding process, the chip and the lead were connected electrically by means of bonding wires such as gold (Au) wires, copper (Cu) wires or aluminum (Al) wires, then molding the chip and bonding wires in a package by molded resin for protecting the semiconductor from damping, contamination or damage.

With increasing demands of enhancing function and speed for the electronic products, there is a constant pressure to build and pack more circuit elements in the IC. The size of the chip thus becomes bigger. However one of the contemporary design requirements for electronic products need slim size and light weight. Hence wafer producers are under great pressure to increase circuit density in IC

chip including more function but without increasing the IC dimension. The chip package also has to meet this trend of slim size and light weight for saving space in the circuit board for semiconductor devices. Numerous package techniques and methods have been proposed for meeting this requirement.

FIGS. 1A and **1B** illustrate a conventional semiconductor package method named quad flat non-leaded (QFN) package. The chip **1** is adhered to a die pad **32** located on a prefabricated lead frame **3** by silver paste **2**, and the chip **1** is connected to a lead **31** through bonding wires **5** in wire bonding process. Thereafter, a molding process is performed. As the QFN package has only a half covered by molded resin **6**, said lead **31** exposed outside the bottom side of the lead frame **3** is prone to form a flash **7** after the molding process. As a result, the subsequent manufacturing processes might be adversely affected.

For preventing the flash **7** from taking place, a conventional method is to adhere a high-temperature-resistant tape **8** to the bottom side of the lead frame **3** (shown in **FIG. 2A**). After the wire bonding process, the lead frame **3** stuck with the tape **8** is transported to the molding process. When the molding process is finished and the molded resin **6** is solidified, the tape **8** is removed (shown in **FIG. 2B**). This method needs additional steps of adhering the tape **8** to the lead frame **3** and removing the tape **8** later. This additional process makes production cost higher. Furthermore, as the tape **8** is a pliable material without hard and rigid property, it

has a buffer effect on the lead frame **3** during wire bonding process, such as in thermo sonic (T/S) process or thermo compress (T/C) process, and may result in not even transmission of bonding force. Consequently, the bonding force might be negatively impacted and result in dropping of bondability.

FIG. 3 depicts another common problem happened to conventional wire bonding process. During the process, the lead frame **3** is placed on a heat block **9** and is held thereon by a window clamp **10** at the upper side for holding the lead **31** securely. Then the upper side of the chip **1** and the lead **31** are electrically connected by bonding wires **5** at two ends thereof. As the lead **31** of the QFN package product generally has a smaller surface and finer pitch, it is more difficult to securely hold the lead **31** between the heat block **9** and window clamp **10** during wire bonding process. The lead **31** tends to vibrate during the wire bonding process and may result in poorer bondability.

Moreover, every product needs a unique lead frame **3** for supporting and wiring the chip **1**. It takes more time and cost in design and production. The lead frame **3** also takes considerable size and height in a finished package. This becomes another concern in designing slim and light products.

U.S. Pat. No. 5,869,905 discloses a semiconductor package structure which omits the lead frame for saving the package height. It includes a substrate which has a surface larger than the chip. The substrate has a through-hole for holding the back side of the chip on

the substrate by vacuum suction force through the through-hole. In wire bonding process, the upper side of the chip and the substrate are connected by bonding wires. After the molding process in which the chip and bonding wires are encapsulated by a molding compound, the perforated substrate is removed for getting a package which has the bonding wires exposed directly to the surface of the molding compound.

Because of no substrate, the U.S. Pat. 5,869,905 package has a smaller size. However it still has the following disadvantages:

1. Holding the chip by vacuum suction force needs high precision equipment. A slight surface defect or not smoothness on the chip could cause chip displacement and may affect subsequent wire bonding process.

2. During wire bonding process, the bonding wires are directly soldered to the surface of the substrate, but the chip and substrate are not permanently engaged with each other (i.e. a temporarily engagement by vacuum force). The chip and substrate are easy to produce relative displacement when subject to an external force. This may cause break down of the bonding wire joints and form a flash in molding process.

3. The package loses a significant heat dissipating channel because of the omission of the lead frame.

4. The bonding wires are exposed to the surface of the molded resin after the package is completed. The exposed bonding wire is too small and is difficult for soldering on a circuit board in

subsequent processes. To increase the soldering size will need additional process after the package is finished which will result in higher cost.

SUMMARY OF THE INVENTION

In view of the foregoing disadvantages, it is therefore an object of this invention to provide a structure and production method for semiconductor package which has no substrate so that flash may be prevented from happening to the exposed lead.

It is another object of this invention to eliminate the adhesive tape for improving the flash phenomenon and to provide a higher rigid substrate for wire bonding process, so that the bonding force may be fully transmitted to increase bondability.

It is a further object of this invention to provide a thin lead layer to replace conventional lead frame for engaging with a substrate to reduce total package thickness, and to hold the chip without the conventional clamping means so that the chip and lead won't vibrate during wire bonding process, and the package may has a heat dissipating channel to facilitate subsequent manufacturing processes.

It is yet another object of this invention to provide a simple structure and method for improving the packaging process, and enhancing product quality and production yield.

In order to achieve aforesaid objects, this invention provides an interim substrate covered by a solder mask at selected areas. The surface of the interim substrate that are not covered by the solder

mask have a plurality of lead layers and die pad layers formed thereon at selected locations. The interim substrate provides a firm support base for bonding wires soldering on the lead layers during wire bonding process. After molding process is completed, and singulation processes are finished, the interim substrate is removed by etching process.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention, as well as its many advantages, may be further understood by the following detailed description and drawings, in which:

FIG. 1A and **1B** are schematic views of a conventional semiconductor package structure, with an enlarged fragmentary view of flash phenomenon.

FIG. 2A and **2B** are schematic views of a conventional scheme for preventing flash.

FIG. 3 is a schematic view of a conventional scheme for holding the lead.

FIG. 4 is the process flow chart of this invention.

FIG. 5A through **5H** are schematic views of the process steps of this invention.

FIG. 6 is a schematic view of another embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to **FIG. 4**, the process according to the method of this invention includes the following steps: set up an interim substrate of

a selected thickness made of copper; coat the surface of the interim substrate with a solder mask which is a layer of polyimide or ultraviolet (UV)-curable resin; perform photolithography process on the coated substrate to form a patterned solder mask; plate the interim substrate with conductive materials such as nickel (Ni) and gold to form a lead layer and a die pad layer; perform die bonding, wire bonding and molding processes; singulate the package; and etch the interim substrate to get a semiconductor package without substrate.

FIGS. 5A through **5H** illustrate the embodiment of the process steps set forth above. Referring to **FIG. 5A**, prepare an interim substrate **11** by selecting a copper of a desired thickness which has a flat surface. Referring to **FIG. 5B**, coat and cover the surface of the interim substrate **11** with a layer of photosensitive insulation material of a selected thickness such as polyimide or UV-curable resin to form a blank solder mask **12** thereon. Referring to **FIG. 5C**, perform photolithography process by projecting UV light through a mask which has selected circuit patterns upon the blank solder mask **12**. After photography developing process, the solder mask **12** will cover only selected areas of the surface of the interim substrate **11**, and the non-covered areas are exposed to the surface of the interim substrate **11**. Referring to **FIG. 5D**, evenly form a lead layer **13** and a die pad layer **14** on the exposed surface areas of the interim substrate **11** by plating conductive materials such as nickel and gold. The lead layer **13** and die pad layer **14** have respectively a smaller

thickness than the solder mask **12**. Referring to **FIG. 5E**, perform die bonding process by adhering the back side of the chip **1** with silver paste **2** for sticking to the surface of the die pad layer **14**, then perform wire bonding process for soldering the upper sides of the chip **1** and lead layer **13** with a bonding wire **5** made of gold, copper or aluminum to establish electrical connection between the chip **1** and lead layer **13**. Referring to **FIG. 5F**, encapsulate the chip **1**, die pad layer **14**, solder mask **12**, lead layer **13** and bonding wires **5** with molded resin **6**, and solidify the resin to form a package through molding process. Referring to **FIG. 5G**, singulate package by means of cutting tools **15** along a preset street into the solidified molded resin **6** to a selected depth below the top surface of the interim substrate **11** without hurting the chip **1** and bonding wires **5**, the singulated package remains on the interim substrate **11**. Referring to **FIG. 5H**, remove the copper-based interim substrate **11** by etching process and expose the solder mask **12**, lead layer **13** and die pad layer **14** to the bottom surface of the package for forming the finished semiconductor package without substrate.

FIG. 6 depicts another embodiment of this invention which is largely constructed and produced like the one shown in **FIGS. 5A** through **5H**. However during the solder mask **12** formation process, the photo mask pattern used in the photolithography process is changed for forming the solder mask **12** on the area previously reserved for the die pad layer **14** (the solder mask **12** is produced like the one set forth above, thus will be omitted herein). The lead

layer **13** remains the same. The chip **1** is adhered to the surface of the solder mask **12** by silver paste **2**. By similar molding process to encapsulate the chip **1**, solder mask **12**, lead layer **13** and bonding wires **5** with molded resin **6**, and singulation process to expose the solder mask **12** and lead layer **13** to the bottom surface of the package, a semiconductor package without substrate may be obtained.

In the wire bonding process set forth above, the existing of the copper-based interim substrate **11** may provide the lead layer **13** a firm metal support base. Hence the bonding force occurred during the wire bonding process can be transmitted fully and effectively. The chip **1** may also be held securely on the interim substrate **11** without producing displacement when subject to external force. The wire bonding process thus may proceed steadily with higher bondability. Furthermore, during the molding process, because the solder mask **12**, lead layer **13** and die pad layer **14** are tightly engaged with the interim substrate **11**, the molded resin **6** may be prevented from spilling over to the bottom surface of the lead layer **13** and die pad layer **14**, thus the flash phenomenon may be avoided. In addition, the lead layer **13** and die pad layer **14** are formed on the surface of the interim substrate **11** by plating of gold and nickel, their thickness is smaller than conventional lead frame. They also provide a heat dissipating channel. In the structure of this invention, the lead layer **13** is exposed to the bottom surface of the whole semiconductor package and may provide surface area needed for

subsequent process of soldering to the circuit substrate.

It may thus be seen that the objects of the present invention set forth herein, as well as those made apparent from the foregoing description, are efficiently attained. While the preferred embodiments of the invention have been set forth for purpose of disclosure, modifications of the disclosed embodiments of the invention as well as other embodiments thereof may occur to those skilled in the art. Accordingly, the appended claims are intended to cover all embodiments which do not depart from the spirit and scope of the invention.